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Izolacijski vmesnik s kapacitivno bariero in postopek prenosa signala s pomočjo takega izolacijskega vmesnika

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Izolacijski vmesnik s kapacitivno bariero in postopek prenosa signala s pomočjo takega izolacijskega vmesnika

Izum se nanaša na izolacijski vmesnik s kapacitivno bariero, ki na vhodni strani kapacitivne bariere obsega vhodno vezje z diferenčnima izhodoma za prvi in drugi logični izhodni signal, ki sta komplementarna drug drugemu in sta repliki prenašanega vhodnega signala, in prvi in drugi barierni kondenzator za omenjeni prvi oziroma drugi logični izhodni signal in na izhodni strani kapacitivne bariere izhodno vezje z vhodom za prvi in drugi preko kapacitivne bariere prenešeni logični signal, to pa obsega prvi in drugi napetostni primerjalnik. Izum se nanaša tudi na postopek prenosa signala s pomočjo takega izolacijskega vmesnika.

Izum je po mednarodni klasifikaciji patentov uvrščen v razred H 03F 03/38.

Izum rešuje tehnični problem, poiskati takšen cenen izolacijski vmesnik s kapacitivno bariero in postopek prenosa signala s pomočjo takšnega izolacijskega

vmesnika, da bo med vezjema na vhodni in izhodni strani kapacitivne bariere omogočen tudi najhitrejši prenos podatkov, pri čemer se bo v vezju na vhodni strani oblikoval za vezje na izhodni strani najprimernejši vhodni signal in bo prenos neobčutljiv na zelo hitro spreminjanje razlike električnega potenciala med napajanjima omenjenih vhodnega in izhodnega vezja celo v razredu 10 kV/μs, obenem pa naj bo izolacijski vmesnik s kapacitivno bariero izpopolnjen, tako da bo sprejemno vezje prišlo v pravilno logično stanje takoj po vklopu le-tega in bo ostalo v pravilnem logičnem stanju tudi potem, ko dalj časa ni prišlo do spremembe izhodnega signala v vezju na vhodni strani kapacitivne bariere.

Izolacijski vmesnik omogoča prenos podatkov, običajno v digitalni obliki, med dvema ali več vezji, ki imajo ločene vire napajalne napetosti. Ker nimajo skupne točke ozemljitve, med vezji nastane napetostna razlika, ki lahko doseže tudi nekaj kilovoltov in se lahko zelo hitro spreminja, tako da hitrost spreminjanja napetostne razlike doseže red velikosti 10 kV/μs.

V izolacijskih vmesnikih se izenačevalni električni tokovi med vezji preprečujejo s sredstvi, ki temeljijo na različnih fizikalnih osnovah.

Daleč najbolj razširjen je optični izolacijski vmesnik. V vhodnem vezju fotodioda pretvori električen signal v svetlobne impulze, ki jih bipolarni tranzistor v izhodnem vezju pretvori nazaj v električen signal. Razen v visokem cenovnem razredu optični izolacijski vmesnik omogoča le sorazmerno nizko hitrost prenosa podatkov v višini nekaj megahertzov, omenjena njegova elementa pa imata precej visoko porabo električnega toka.

Hitro se uveljavlja vmesnik na magnetni sklop magnetne zanke in tipala magnetnega polja. Ugodno je, da se magnetni sklop lahko izvede na enotnem substratu integriranega vezja; tokovna zanka je prevodna sled, ki je s plastjo silicijevega oksida ločena od elementov, ki so priključeni na drugo napajanje, tipalo pa je magnetno-uporovni element. Omogoča prenos podatkov s hitrostjo do 50 MHz. Pri ustrezni konstrukciji potrebuje mnogo manjši tok kot optični izolacijski vmesnik. Izdeluje pa se po relativno zahtevni tehnologiji, saj se magnetno-uporovni element na integrirano vezje doda z zahtevnimi in dragimi tehnološkimi koraki.

Poznani so tudi izolacijski vmesniki na kapacitivni sklop. V osnovni izvedbi se protifazna digitalna izhodna signala U1o± vhodnega vezja A1', ki sta repliki prenašanega vhodnega signala Ui, vodita na prvo ploščo bariernih kondenzatorjev C'± (sl. 1). Z njune druge plošče se vodita digitalna vhodna signala U2i± v izhodno vezje A2', na katerega izhodu se pojavi prenašani signal Uout . Visok in nizek potencial vira napajalne napetosti vhodnega vezja A1' sta U1+ oziroma U1- in enako U2+ oziroma U2- pri izhodnem vezju A2'. Druga plošča bariernih kondenzatorjev C'± je preko kondenzatorja C"± kot tudi preko upora R'±, pri čemer vsaka od povezav predstavlja napetostni delilnik, in sicer prva za spremenljiv in druga za enosmeren signal, priključena na sredinski potencial vira napajalne napetosti izhodnega vezja A2'. Časovni potek napetosti vhodnega signala Ui glede na ta sredinski potencial je prikazan v prvem oknu na sl. 2; ob t=90 ns je začela naraščati potencialna razlika med napajalnim virom prvega vezja A1' in napajalnim virom drugega vezja A2', ki se odrazi kot napetost na kondenzatorjih C'+ in C'-, in je dosegla vrednost 50 V. S polno črto in črtkano sta v drugem in tretjem oknu na sl. 2 prikazana časovna poteka protifaznih signalov U1o± oziroma U2i±. V četrtem oknu na sl. 2 pa je prikazan prenešeni izhodni signal Uout, ki je po frekvenci enak vhodnemu signalu Ui. Enosmerne in nizkofrekvenčne potencialne razlike so po višini omejene le s prebojno

trdnostjo kondenzatorjev C'+ in C'-. Upora R'± zagotavljata, da sta po velikosti vhodna signala U2i± tudi pri nizkih frekvencah vedno znotraj območja dovoljenih vhodnih napetosti napetostnih primerjalnikov v vezju A2'. V številnih uporabah pa mora opisani vmesnik delovati tudi pri hitrem spreminjanju potencialne razlike med napajalnim virom prvega vezja A1' in napajalnim virom drugega vezja A2'. Potrebno zmanjšanje visokofrekvenčnih signalov U2i± se doseže s primernim razmerjem kapacitet kondenzatorjev C'+ in C"+ oziroma C'- in C"-. To razmerje mora biti 1:500, če naj opisani vmesnik prenese potencialno razliko 1 kV pri dovoljeni vhodni napetosti napetostnega primerjalnika v višini 2 V. Tolikšno razmerje pa zmanjša tudi amplitudo signalnih replik U2i± vhodnega signala Ui na vhodu v vezje A2' na le nekaj milivoltov. To hitrost prenosa signala upočasni ali celo onemogoči, saj so amplitude signalov že v območju značilnih napetosti ničenja napetostnega primerjalnika. Ob zagotovitvi neobčutljivosti na hitro spreminjanje potencialne razlike med napajalnim viroma se z opisanim vmesnikom torej ne more hkrati zagotoviti najhitrejši možen prenos podatkov.

V patentnem spisu US 4.835.486 je sicer opisan vmesnik na kapacitiven sklop, ki je primeren za prenos digitalnih signalov do frekvence navzgor do 1,5 MHz. Uporablja odvajalni sklop na kapacitivni barieri, vendar časovna konstanta odvajalnega sklopa znaša 9 ns. Časovna konstanta je torej daljša od značilnega časa trajanja spremembe signalne replike na izhodu iz prvega vezja pred kapacitivno bariero, zato se mora amplituda signalne replike na vhodu v vezje za kapacitivno bariero omejiti z diodnim omejevalnikom. Nadalje vhodni ojačevalnik v vezju za kapacitivno bariero pretvori vhodni signalni par v en sam signal. S tem se dodatno popači širina impulzov , saj nikoli ni možno zagotoviti popolno simetrijo spreminjanja ojačevalnikovega izhodnega signala.

Izolacijskemu vmesniku na kapacitiven sklop pa je imanentna omejitev, da zaradi kapacitivne bariere ne more prenašati časovno nespremenljive informacije. Zato se po vklopu ali pa potem, ko dalj časa ni prišlo do spremembe izhodnega signala v vezju na vhodni strani kapacitivne bariere, šele po prvi spremembi logičnega stanja izhodnega signala vezja na vhodni strani kapacitivne bariere vhodni signal v vezju na izhodni strani kapacitivne bariere postavi v pravilno logično stanje, to se pravi v logično stanje omenjenega izhodnega signala.

Navedeni tehnični problem je rešen z izolacijskim vmesnikom s kapacitivno bariero, ki obsega

- na vhodni strani kapacitivne bariere vhodno vezje z diferenčnima izhodoma za prvi in drugi logični izhodni signal, ki sta repliki prenašanega vhodnega signala in sta komplementarna drug drugemu,
- prvi in drugi barierni kondenzator za prvi oziroma drugi logični signal in
- na izhodni strani kapacitivne bariere izhodno vezje z vhodom za prvi in drugi logični vhodni signal, ki sta komplementarna drug drugemu, obsegajoče prvi in drugi napetostni primerjalnik,

pri čemer je izolacijski vmesnik po izumu s kapacitivno bariero značilen po tem,

da sta v vhodnem vezju predvidena prvi integrirni sklop in drugi integrirni sklop, preko katerih sta se vodila prvi logični izhodni signal oziroma drugi logični izhodni signal in s katerih časovnima konstantama so se nastavile strmine bokov signalov oziroma časi naraščanja in padanja signalov,

in da je na izhodno sponko prvega bariernega kondenzatorja in drugega bariernega kondenzatorja na eni strani in na sponko sredinskega potenciala izhodnega vezja na drugi strani priključen takšen prvi upor oziroma drugi upor,

da sta časovna konstanta prvega odvajalnega sklopa iz prvega bariernega kondenzatorja in prvega upora

in časovna konstanta drugega odvajalnega sklopa iz drugega bariernega kondenzatorja in drugega upora
manjši od časov naraščanja in padanja logičnih izhodnih signalov kot replik prenašanega signala.

Izolacijski vmesnik po izumu s kapacitivno bariero je nadalje značilen po tem, da se prvi logični vhodni signal in drugi logični vhodni signal izhodnega vezja vodita neposredno na prvi oziroma drugi vhod prvega napetostnega primerjalnika in neposredno na drugi oziroma prvi vhod drugega napetostnega primerjalnika in da sta izhod prvega napetostnega primerjalnika in izhod drugega napetostnega primerjalnika priključena na vhoda flipflopa, katerega izhod je izhod izolacijskega vmesnika s kapacitivno bariero.

Izolacijski vmesnik s kapacitivno bariero je po izumu izpopolnjen, tako da je vhod osnovnega izolacijskega vmesnika s kapacitivno bariero priključen na krmilni vhod impulzno-širinskega modulatorja, na katerega drugi vhod se neprekinjeno dovaja signal stalne frekvence in katerega izhod je priključen na vhod pomožnega izolacijskega vmesnika za prenos po pomožnem komunikacijskem kanalu, in da sta izhod osnovnega izolacijskega vmesnika s kapacitivno bariero in izhod pomožnega izolacijskega vmesnika za prenos po pomožnem komunikacijskem kanalu priključena na vhoda odločitvenega logičnega vezja, ki skrbi za pravilno logično stanje prenešenega signala, in da je izhod odločitvenega logičnega vezja izhod izpopolnjenega izolacijskega vmesnika s kapacitivno bariero.

Izpopolnjeni izolacijski vmesnik s kapacitivno bariero je nadalje značilen po tem, da se glede na prisotnost moduliranega signala na izhodu pomožnega izolacijskega vmesnika za prenos po pomožnem komunikacijskem kanalu vklap-

ljajo ali izklapljajo posamezni sklopi na izhodni strani osnovnega izolacijskega vmesnika s kapacitivno bariero.

Navedeni tehnični problem je rešen tudi s postopkom po izumu za prenos signala skozi izolacijski vmesnik s kapacitivno bariero, pri čemer je omenjeni postopek značilen po tem, da se v vhodnem vezju izolacijskega vmesnika s kapacitivno bariero z integriranjem s primerno časovno konstanto nastavi strmina bokov oziroma časi naraščanja in padanja signalnih replik prenašanega signala in da se omenjeni signalni repliki odvajata na prvem odvajalnem sklopu oziroma drugem odvajalnem sklopu kapacitivne bariere in da sta časovni konstanti prvega in drugega odvajalnega sklopa manjši od časov naraščanja in padanja signalnih replik prenašanega signala.

Postopek po izumu za prenos signalov skozi izolacijski vmesnik s kapacitivno bariero je nadalje značilen po tem, da se signala na odvajalnih sklopih kapacitivne bariere tvorjenih odvodov vodita neposredno na vhode dveh napetostnih primerjalnikov v izhodnem vezju izolacijskega vmesnika s kapacitivno bariero.

Z izumom izpopolnjeni postopek prenosa signalov skozi izolacijski vmesnik s kapacitivno bariero pa je značilen po tem, da se poleg prenosa vhodnega signala skozi osnovni izolacijski vmesnik s kapacitivno bariero skozi pomožen izolacijski vmesnik za prenos po pomožnem komunikacijskem kanalu neprekinjeno opravlja prenos z vhodnim signalom impulzno-širinsko moduliranega signala stalne frekvence in da se glede na modulacijo prenešenega impulzno-širinsko moduliranega signala naravnava logično stanje z izolacijskim vmesnikom s kapacitivno bariero prenešenega signala.

V nadaljnjem bo izum podrobno obrazložen in predstavljene bodo številne dosežene prednosti, in sicer na osnovi opisa izvedbenega primera izolacijskega vmesnika s kapacitivno bariero in s pomočjo tega vmesnika izvajanega postopka prenosa signala ter pripadajočega načrta oziroma grafov, ki prikazujejo na

sl. 3 shematski prikaz z izumom izpopolnjenega izolacijskega vmesnika, v katerem sta osnovnemu izolacijskemu vmesniku po izumu s kapacitivno bariero priključena impulzno-širinski modulator in pomožen izolacijski vmesnik za prenos z vhodnim signalom impulzno-širinsko moduliranega signala stalne frekvence zaradi prenašanja informacije o logičnem stanju prenašanega signala;

sl. 4 časovni potek vhodnega signala in časovni potek na izolacijskem vmesniku po izumu s kapacitivno bariero doseženih signalnih replik vhodnega signala s strmino 1 V/ns bokov pred in za odvajalnim sklopom ter izhodnega signala;

sl. 5 časovni potek istih signalov kot na sl. 4 pri strmini 12 V/ns bokov signalnih replik vhodnega signala.

Osnovni izolacijski vmesnik po izumu s kapacitivno bariero je v poenostavljeni obliki prikazan kot del vezja na sl. 3. Obsega naslednje sklope.

- Na vhodni strani kapacitivne bariere je vhodno vezje A1 z diferenčnima izhodoma za prvi in drugi logični izhodni signal U1o+ oziroma U1o-, ki sta repliki prenašanega vhodnega signala Ui in sta komplementarna drug drugemu. V vhodnem vezju A1 sta predvidena prvi integrirni sklop (R1, C1)+ in drugi integrirni sklop (R1, C1)-, preko katerih se vodita prvi logični izhodni signal U1o+ oziroma drugi logični izhodni signal U1o-. S časovnima konstantama integrirnih sklopov (R1, C1)± se nastavijo strmine bokov signalov U1o± oziroma časi naraščanja in padanja signalov U1o±.

- Sledita prvi barierni kondenzator C+ in drugi barierni kondenzator C-, na katera se vodi prvi logični signal U1o+ oziroma drugi logični signal U1o- in na katerih izhodno sponko na eni strani in na sponko sredinskega potenciala izhodnega vezja A2 na drugi strani je priključen takšen prvi upor R+ oziroma takšen drugi upor R-, da sta časovna konstanta prvega odvajalnega sklopa (C+, R+) iz prvega bariernega kondenzatorja C+ in prvega upora R+ in časovna konstanta drugega odvajalnega sklopa (C-, R-) iz drugega bariernega kondenzatorja C- in drugega upora R- manjši od časov naraščanja in padanja logičnih izhodnih signalov U1o+ in U1o- kot replik prenašanega signala Ui. V predlaganem izolacijskem vmesniku za prenos digitalnega signala s frekvenco do 100 MHz sta torej časovni konstanti prvega in drugega odvajalnega sklopa reda velikosti 1 ns ali celo manj. Na prvem odvajalnem sklopu (C+, R+) se signal U1o+ preslika v signal U2i+, na drugem odvajalnem sklopu (C-, R-) pa signal U1o- v signal U2i-. Tudi signala U2i± sta komplementarna drug drugemu.

- Na izhodni strani kapacitivne bariere je izhodno vezje A2 z vhodom za prvi logični vhodni signal U2i+ oziroma drugi logični vhodni signal U2i-. Izhodno vezje A2 obsega prvi napetostni primerjalnik Co+ in drugi napetostni primerjalnik Co-.

Zgornji in spodnji potencial napetostnega vira za napajanje vhodnega vezja A1 sta U1±, napetostnega vira za napajanje izhodnega vezja A2 pa U2±.

Po izumu se torej časovni konstanti integrirnih sklopov (R1, C1)± izbereta tako, da se nastavijo strmine bokov izhodnih signalov U1o± oziroma časi naraščanja in padanja izhodnih signalov U1o±, da so ti časi daljši od časovnih konstant prvega oziroma drugega odvajalnega sklopa, ki pa naj bosta reda velikosti 1 ns ali celo manj.

S tem da se kontrolira strmina bokov izhodnih signalov U1o± vezja A1, se namreč kontrolirata amplituda in čas trajanja vhodnih signalov U2i± vezja A2. Iz signalov U1o± s položnejšimi boki, na primer s strmino 1 V/ns na sl. 4, nastaneta nižja in dalj časa trajajoča signala U2i±. In obratno, iz signalov U1o± z bolj strmimi boki, na primer s strmino 12 V/ns na sl. 5, nastaneta višja in kratkotrajna signala U2i±.

Na sl. 4 in 5 sta za strmino bokov 1 V/ns oziroma 12 V/ns v prvih dveh oknih prikazana časovni potek vhodnega signala Ui in izhodnih signalov U1o± vezja A1 in sta v drugih dveh oknih prikazana časovni potek vhodnih signalov U2i± vezja A2 in izhodnega signala Uout vezja A2. Ob t=90 ns je začela naraščati potencialna razlika med napajalnim virom prvega vezja A1 in napajalnim virom drugega vezja A2 in je ob t=150 ns dosegla vrednost 50 V. Vhodna signala U2i± vezja A2 (tretje okno) imata impulze z višino okoli 50 mV in trajanjem okoli 10 ns pri 1 V/ns vrednosti strmine bokov signalov U1o± (sl. 4) in impulze z višino okoli 600 mV in trajanjem okoli 1 ns pri 12 V/ns vrednosti strmine bokov signalov U1o± (sl. 5).

V izhodnem vezju A2 se prvi logični vhodni signal U2i+ in drugi logični vhodni signal U2i- vodita neposredno na prvi oziroma drugi vhod prvega napetostnega primerjalnika Co+ in neposredno na drugi oziroma prvi vhod drugega napetostnega primerjalnika Co-.

Izhod prvega napetostnega primerjalnika Co+ in izhod drugega napetostnega primerjalnika Co- sta priključena na vhoda flipflopa F. Izhod flipflopa F je obenem izhod osnovnega izolacijskega vmesnika po izumu s kapacitivno bariero.

Glede na karakteristike primerjalnikov Co± in tudi glede na zahtevo po največji hitrosti prenosa podatkov ter glede na zahtevo po imunosti na hitro spreminjanje potencialne razlike med napetostnima napajalnima viroma vezij A1 in A2 se na prej predstavljeni način oblikujeta optimalna vhodna signala U2i± za izhodno vezje A2.

Časovna konstanta odvajalnih sklopov (C+, R+) in (C-, R-) pa se izbere glede na predvideno največjo hitrost spreminjanja potencialne razlike med napetostnima napajalnima viroma vezij A1 in A2. Če je ta največja hitrost 10 kV/μs, se morata odvajalna sklopa dimenzionirati tako, da omenjena spreminjajoča se potencialna razlika povzroči enosmerni napetosti na vhodih vezja A2 v območju dovoljenih vrednosti za to vezje. Amplituda signalov U2i± je namreč odvisna le od hitrosti spreminjanja signalov U1o± in ne od njune amplitude.

V izolacijskem vmesniku po izumu s kapacitivno bariero vhodna signala U2i± nikoli ne prekrmilita vezja A2, saj se lahko njuni amplitudi in njuna časa trajanja po izumu v celoti določita izključno le s časi naraščanja in padanja signalov U1o± in s časovnima konstantama prvega in drugega odvajalnega sklopa. V sodobnih podmikrometrskih tehnologijah pa je hitrost spreminjanja signalov v območju od 1 V/ns do 10 V/ns. Časovni konstanti odvajalnih sklopov sta zelo skrajšani in sta prednostno pod eno nanosekundo.

Ker sta amplitudi vhodnih signalov U2i± nastavljivi in zato znani, vezje A2 ne potrebuje ojačevalnikov pred napetostnima primerjalnikoma Co±, kar omogoča, da se izredno natančno - napaka je manjša od 0,5 ns - od vezja A1 do vezja A2 ohranja širina impulzov, saj se z dvema enakima primerjalnikoma Co± sprejemata komplementarna signala U2i± in zato prvi zazna prehod iz stanja 0 v stanje 1 in drugi iz stanja 1 v stanje 0.

Izolacijski vmesnik po izumu s kapacitivno bariero omogoča prenos digitalnih signalov do frekvence 100 MHz, kar glede na stanje tehnike predstavlja izboljšanje za dva velikostna razreda.

Z izolacijskim vmesnikom po izumu s kapacitivno bariero sta rešena dva velika problema prenosa podatkov:

- imun je na hitro spreminjanje potencialne razlike med napetostnima napajalnima viroma vezij A1 in A2 reda velikosti 10 kV/μs, tako da se na vhodnih signalih U2i± odrazi kot nemoteč enosmeren prispevek, manjši od 1 V;
- izključno z obliko medsebojno protifaznih izhodnih signalov U1o± vezja A1 določi obliko vhodnih signalov U2i± v vezje A2.

Na sl. 3 je prikazan po izumu izpopolnjeni izolacijski vmesnik s kapacitivno bariero, ki poleg opisanega osnovnega izolacijskega vmesnika (A1, C+, C-, R+, R-, A2) po izumu s kapacitivno bariero za hiter prenos podatkov po osnovnem kanalu BCC obsega še pomožen izolacijski vmesnik za prenos po pomožnem komunikacijskem kanalu ACC. Kot pomožen izolacijski vmesnik se lahko uporabi opisani izolacijski vmesnik (A1, C+, C-, R+, R-, A2) po izumu s kapacitivno bariero ali pa izolacijski vmesnik z nižjo dosegljivo hitrostjo prenosa podatkov, ki ima zato bistveno nižjo porabo električnega toka.

Vhod osnovnega izolacijskega vmesnika (A1, C+, C-, R+, R-, A2) s kapacitivno bariero je priključen na krmilni vhod impulzno-širinskega modulatorja PWM, na katerega vhod se neprekinjeno, na primer od oscilatorja O, dovaja signal stalne frekvence. Izhodni signal impulzno-širinskega modulatorja PWM, ki je moduliran z vhodnim signalom Ui, ki ga je treba prenašati, se vodi na vhod pomožnega izolacijskega vmesnika za prenos po pomožnem komunikacijskem kanalu ACC.

Na izhodu pomožnega komunikacijskega kanala ACC je stalno prisoten pomožni izhodni signal Uouta. V tem signalu razmerje med časom trajanja visokega logičnega nivoja in časom trajanja nizkega logičnega nivoja ni stalno. Če je vhodni signal Ui v visokem logičnem nivoju, ima izhodni signal Uouta na primer visok logični nivo v daljšem delu periode in nizek logični nivo v krajšem delu periode in obratno, če je vhodni signal Ui v nizkem logičnem nivoju. Stalno prisoten podatek o razmerju med trajanjem visokega in nizkega logičnega nivoja impulzno-širinsko moduliranega signala Uouta stalne frekvence predstavlja informacijo o logičnem stanju signala Ui na vhodu oddajnega dela izpopolnjenega izolacijskega vmesnika s kapacitivno bariero.

Na ta način oddajni del izolacijskega vmesnika sprejemnemu delu na drugi strani izolacijske bariere posreduje pomembno dodatno informacijo. Namreč, podatkovni sprejemni del, ki je glavni porabnik električnega toka v sprejemnem vezju, se lahko izklopi, kadar oddajni del ni aktiven, ali pa se izhod sprejemnega dela ponovno uskladi z omenjeno dodatno informacijo, kadar se vhodni signal Ui dalj časa - od 1 μs do 100 μs - ni spremenil, oziroma takoj po vklopu sprejemni del nastavi pravo logično stanje svojega signala oziroma inicializira izhodni signal sprejemnega dela, čim je ugotovil logično stanje vhodnega signala Ui na oddajnem delu. Za nastavitev pravilnega logičnega stanja izhodnega signala v sprejemnem delu izpopolnjenega izolacijskega vmesnika s kapacitivno bariero torej ni treba čakati na prvo spremembo signala oddajnega dela.

V ta namen sta izhod osnovnega izolacijskega vmesnika (A1, C+, C-, R+, R-, A2) s kapacitivno bariero in izhod pomožnega izolacijskega vmesnika za prenos po pomožnem komunikacijskem kanalu ACC priključena na vhoda odločitvenega logičnega vezja DLC, ki skrbi za pravilno logično stanje prenesenega

signala. Izhod odločitvenega logičnega vezja DLC je izhod izpopolnjenega izolacijskega vmesnika s kapacitivno bariero.

Patentni zahtevki

1. Izolacijski vmesnik s kapacitivno bariero, obsegajoč
- na vhodni strani kapacitivne bariere vhodno vezje (A1) z diferenčnima izhodoma za prvi in drugi logični izhodni signal U1o+ oziroma U1o-, ki sta repliki prenašanega vhodnega signala Ui in sta komplementarna drug drugemu,
- prvi barierni kondenzator (C+) in drugi barierni kondenzator (C-) za prvi logični signal U1o+ oziroma drugi logični signal U1o- in
- na izhodni strani kapacitivne bariere izhodno vezje (A2) z vhodom za prvi logični vhodni signal U2i+ oziroma drugi logični vhodni signal U2i-, ki sta komplementarna drug drugemu, obsegajoče prvi napetostni primerjalnik (Co+) in drugi napetostni primerjalnik (Co-), in
označen s tem,
da sta v vhodnem vezju (A1) predvidena prvi integrirni sklop (R1, C1)+ in drugi integrirni sklop (R1, C1)-, preko katerih sta se vodila prvi logični izhodni signal U1o+ oziroma drugi logični izhodni signal U1o- in s katerih časovnima konstantama so se nastavile strmine bokov signalov U1o± oziroma časi naraščanja in padanja signalov U1o±,
in da je na izhodno sponko prvega bariernega kondenzatorja (C+) in drugega bariernega kondenzatorja (C-) na eni strani in na sponko sredinskega potenciala izhodnega vezja (A2) na drugi strani priključen takšen prvi upor (R+) oziroma drugi upor (R-),
da sta časovna konstanta prvega odvajalnega sklopa (C+, R+) iz prvega bariernega kondenzatorja (C+) in prvega upora (R+)
in časovna konstanta drugega odvajalnega sklopa (C-, R-) iz drugega bariernega kondenzatorja (C-) in drugega upora (R-)
manjši od časov naraščanja in padanja logičnih izhodnih signalov U1o+ in U1o- kot replik prenašanega signala Ui.

2. Izolacijski vmesnik s kapacitivno bariero po zahtevku 1,
označen s tem,
da se prvi logični vhodni signal U2i+ in drugi logični vhodni signal U2i- izhodnega vezja (A2) vodita neposredno na prvi oziroma drugi vhod prvega napetostnega primerjalnika (Co+) in neposredno na drugi oziroma prvi vhod drugega napetostnega primerjalnika (Co-)
in da sta izhod prvega napetostnega primerjalnika (C0+) in izhod drugega napetostnega primerjalnika (C0-) priključena na vhoda flipflopa (F),
katerega izhod je izhod izolacijskega vmesnika s kapacitivno bariero.

3. Izolacijski vmesnik s kapacitivno bariero po zahtevku 1 ali 2,
označen s tem,
da je vhod osnovnega izolacijskega vmesnika (A1, C+, C-, R+, R-, A2) s kapacitivno bariero priključen na krmilni vhod impulzno-širinskega modulatorja (PWM), na katerega drugi vhod se neprekinjeno dovaja signal stalne frekvence in katerega izhod je priključen na vhod pomožnega izolacijskega vmesnika za prenos po pomožnem komunikacijskem kanalu (ACC),
da sta izhod osnovnega izolacijskega vmesnika (A1, C+, C-, R+, R-, A2) s kapacitivno bariero in izhod pomožnega izolacijskega vmesnika za prenos po pomožnem komunikacijskem kanalu (ACC) priključena na vhoda odločitvenega logičnega vezja (DLC), ki skrbi za pravilno logično stanje signala, ki se prenaša z osnovnim izolacijskim vmesnikom (A1, C+, C-, R+, R-, A2) s kapacitivno bariero,
in da je izhod odločitvenega logičnega vezja (DLC) izhod izolacijskega vmesnika s kapacitivno bariero.

4. Izolacijski vmesnik s kapacitivno bariero po zahtevku 3,
označen s tem,

da se glede na stanje moduliranega signala na izhodu pomožnega izolacijskega vmesnika za prenos po pomožnem komunikacijskem kanalu (ACC) vklapljajo ali izklapljajo posamezni sklopi na izhodni strani osnovnega izolacijskega vmesnika (A1, C+, C-, R+, R-, A2) s kapacitivno bariero.

5. Postopek prenosa signala skozi izolacijski vmesnik s kapacitivno bariero, označen s tem,
da se v vhodnem vezju izolacijskega vmesnika s kapacitivno bariero z integriranjem s primerno časovno konstanto nastavi strmina bokov oziroma časi naraščanja in padanja signalnih replik U1o+ in U1o- prenašanega signala Ui
in da se omenjeni signalni repliki U1o+ in U1o- odvajata na prvem odvajalnem sklopu oziroma drugem odvajalnem sklopu kapacitivne bariere,
in da sta časovni konstanti prvega in drugega odvajalnega sklopa vsaj manjši od časov naraščanja in padanja signalnih replik U1o+ in U1o- prenašanega signala Ui.

6. Postopek prenosa signalov skozi izolacijski vmesnik s kapacitivno bariero po zahtevku 5, označen s tem,
da se signala U2i± na odvajalnih sklopih kapacitivne bariere tvorjenih odvodov vodita neposredno na vhode dveh napetostnih primerjalnikov v izhodnem vezju izolacijskega vmesnika s kapacitivno bariero.

7. Postopek prenosa signalov skozi izolacijski vmesnik s kapacitivno bariero po zahtevku 5 ali 6, označen s tem,
da se poleg prenosa vhodnega signala Ui skozi osnovni izolacijski vmesnik s kapacitivno bariero skozi pomožen izolacijski vmesnik za prenos po pomožnem komunikacijskem kanalu (ACC) neprekinjeno opravlja prenos z vhodnim signalom Ui impulzno-širinsko moduliranega signala Uia stalne frekvence

in da se glede na modulacijo prenešenega impulzno-širinsko moduliranega signala Uouta naravnava logično stanje z izolacijskim vmesnikom s kapacitivno bariero prenešenega signala Uout.

Izvleček

Izolacijski vmesnik s kapacitivno bariero in
postopek prenosa signala s pomočjo takega izolacijskega vmesnika

Prenos signala skozi izolacijski vmesnik s kapacitivno bariero poteka tako, da se v vhodnem vezju vmesnika z integriranjem s primerno časovno konstanto nastavi strmina bokov oziroma časi naraščanja in padanja signalnih replik U1o± prenašanega signala in da se omenjeni signalni repliki odvajata vsaka na ustreznem odvajalnem sklopu, pri čemer sta časovni konstanti teh odvajalnih sklopov manjši od časov naraščanja in padanja signalnih replik in sta prednostno reda velikosti nanosekunde ali manj. Vezje na izhodni strani kapacitivne bariere zato ne potrebuje ojačevalnika pred napetostnima primerjalnikoma, kar omogoča, da se izredno natančno ohranja širina impulzov. Prenos podatkov je imun na hitro spreminjanje potencialne razlike med napetostnima napajalnima viroma vhodnega in izhodnega vezja v redu velikosti 10 kV/μs. Z izumom se omogoča prenos digitalnih signalov do frekvence 100 MHz.

(Sl. 5)

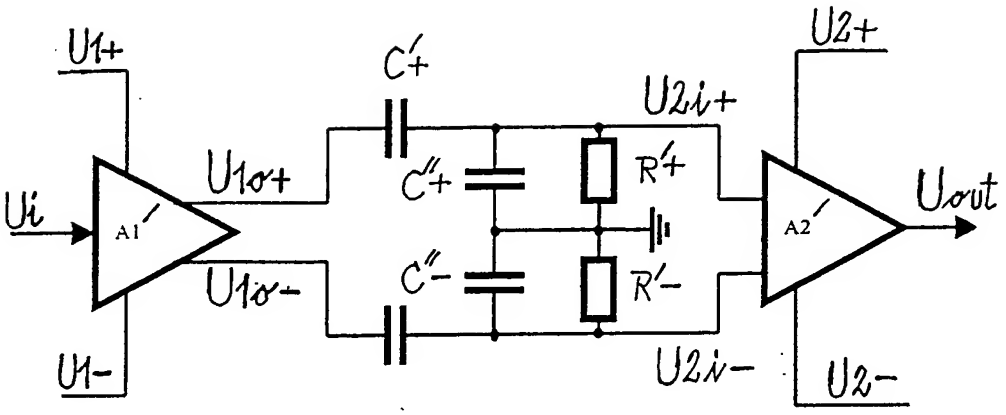
U1+
U1-
Ui
A1
U1o+
U1o-
C'+
C''+
C''-
R'+
R'-
U2i+
U2i-
A2
U2+
U2-
Uout

Fig. 1

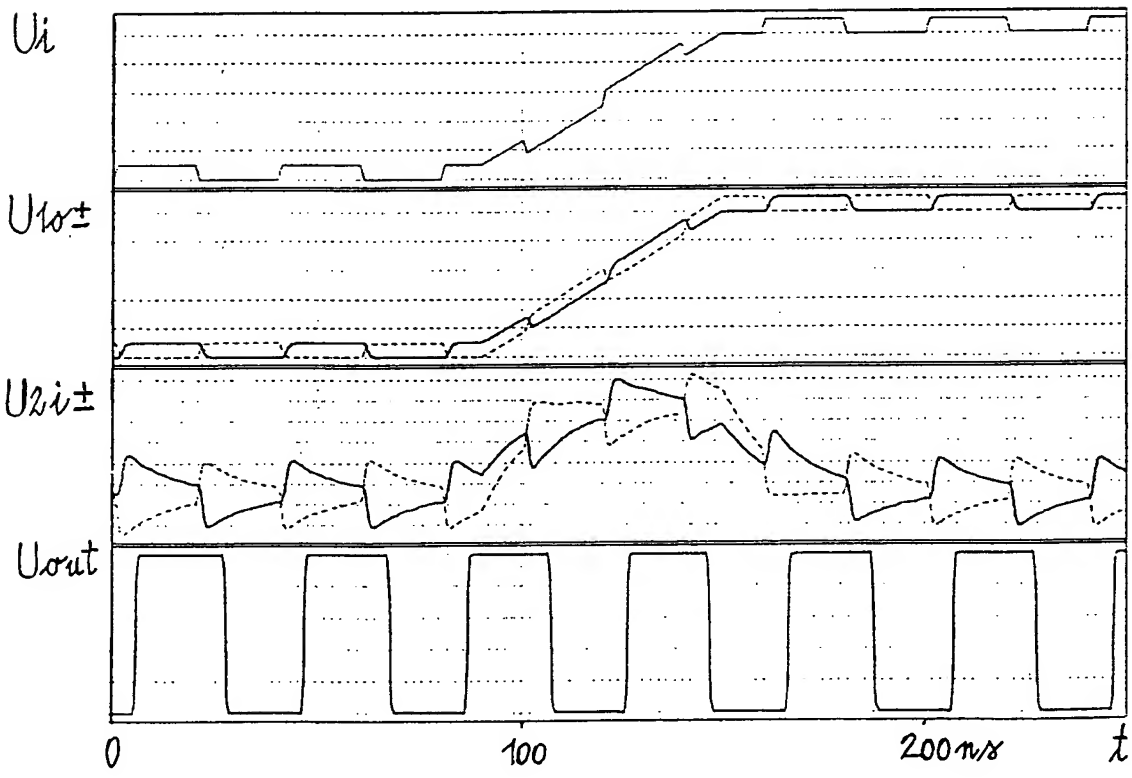
Ui
U1o±
U2i±
Uout
0
100
200 n/s
t

Fig. 2

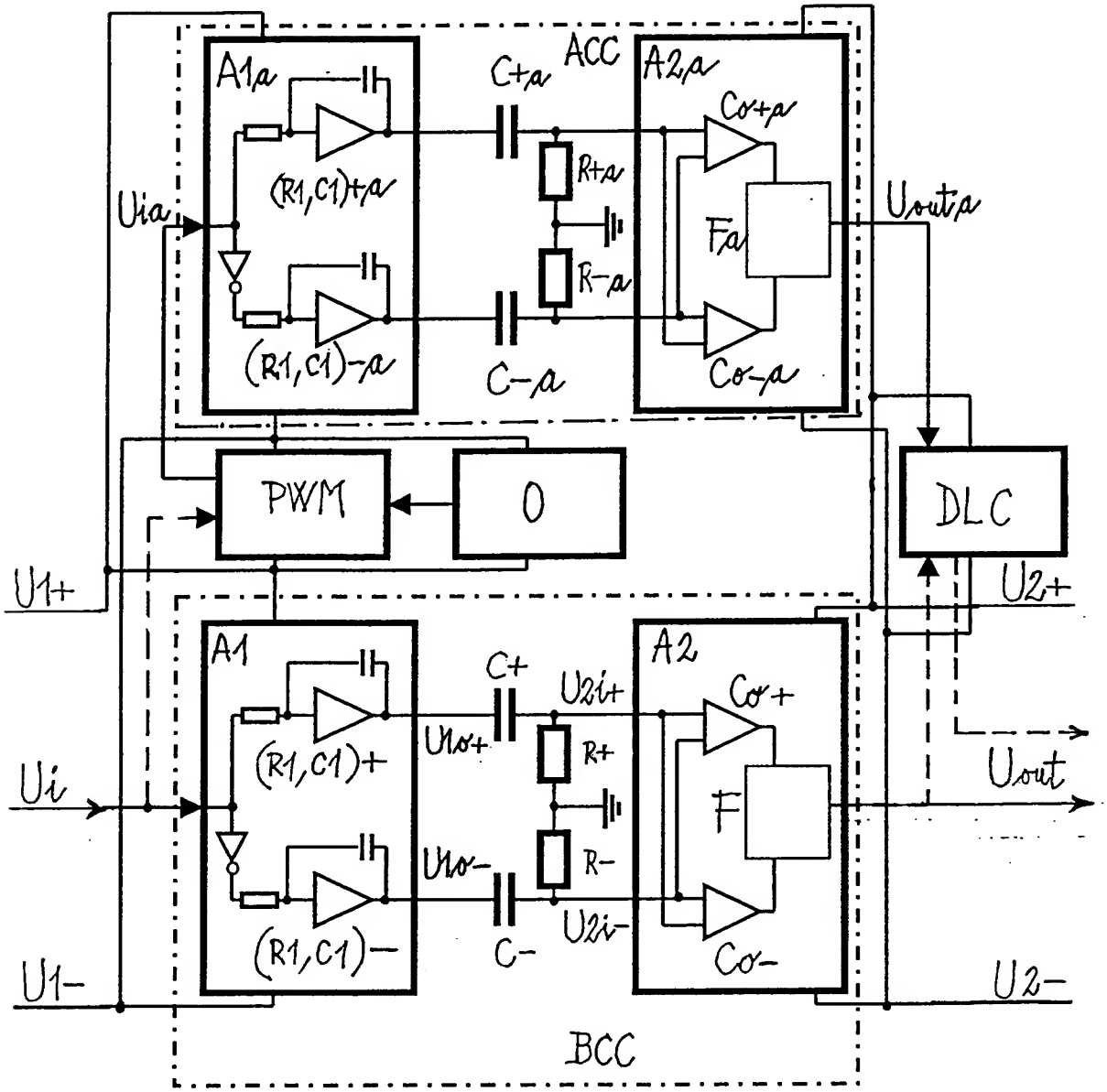
ACC
A1a
(R1,C1)+a
(R1,C1)-a
C+a
C-a
R+a
R-a
A2a
Co+a
Co-a
Fa
Uia
Uout a
PWM
0
DLC
U1+
U2+
A1
(R1,C1)+
(R1,C1)-
C+
C-
U1o+
U1o-
U2i+
U2i-
R+
R-
A2
Co+
Co-
F
Ui
Uout
U1-
U2-
BCC

Fig. 3

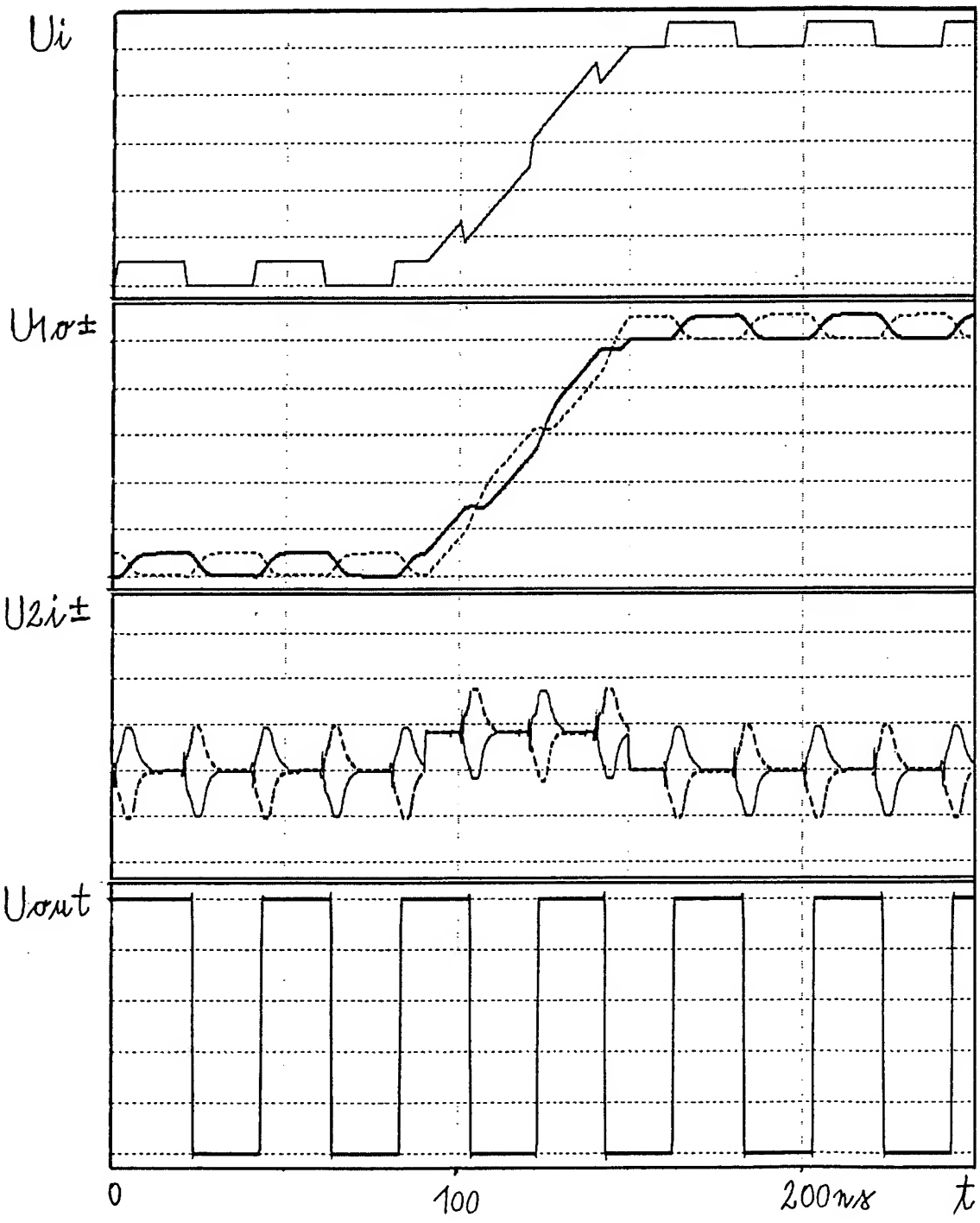

Fig. 4

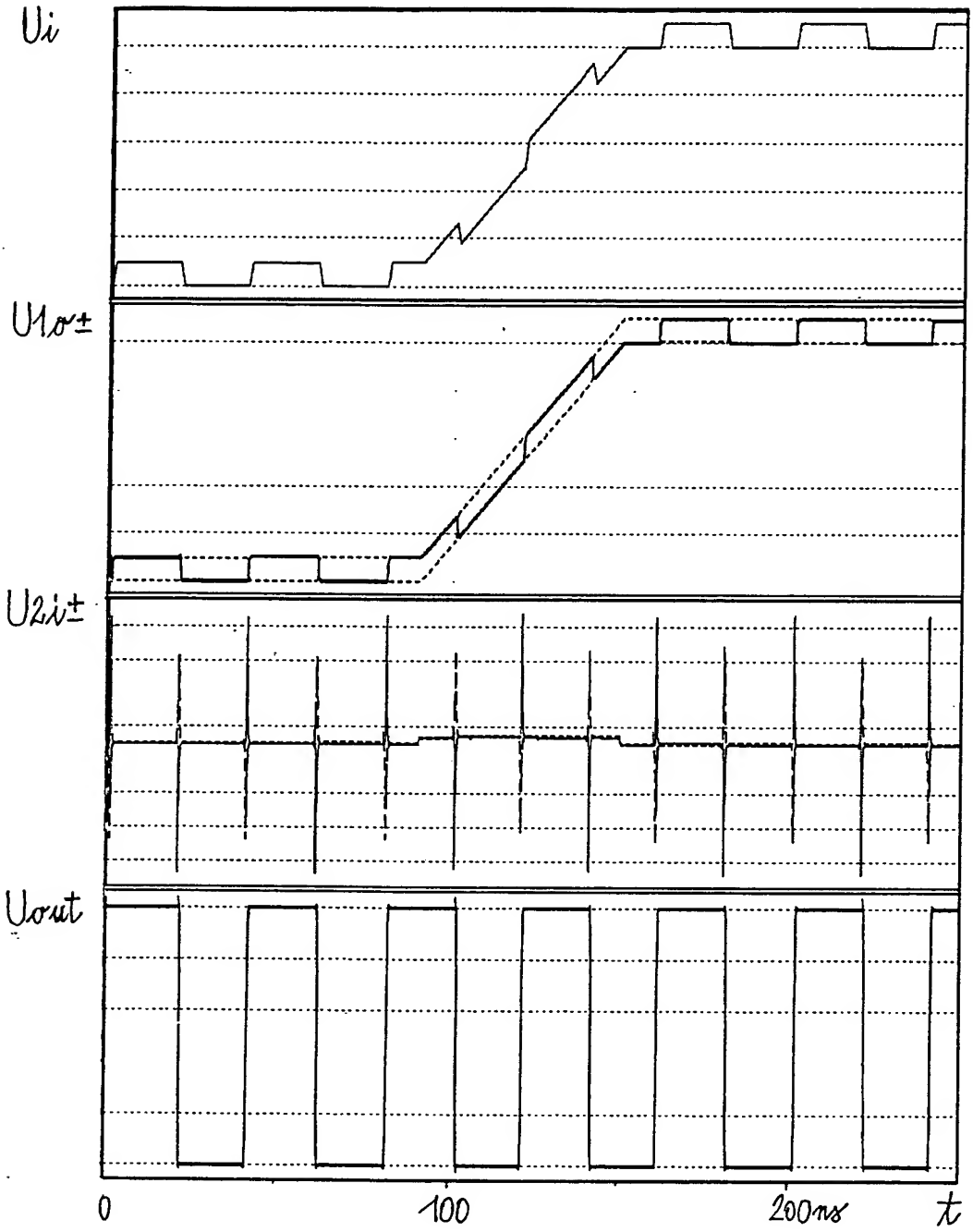

Fig. 5

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CERTIFICATE

Slovenian Intellectual Property Office hereby certifies that the document annexed hereto is a true copy of the patent application, as follows:

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Isolation interface with capacitive barrier and method for transmitting a signal by means of such isolation interface

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(signed) Jovan Malešević, Advisor

(rubber stamp)

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Isolation interface with capacitive barrier and method for transmitting a signal by means of such isolation interface

The present invention relates to an isolation interface with a capacitive barrier comprising, at the input end of the capacitive barrier, an input circuit with differential outputs for a first and a second logical output signals that are complementary to one another and are replicas of a transmitted input signal, and a first and a second barrier capacitors for the first and the second logical signals, respectively, and, at the output end of the capacitive barrier, an output circuit with inputs for a first and a second logical signal transmitted across the capacitive barrier, the said output circuit comprising a first and a second voltage comparators. The present invention also relates to a method for transmitting a signal by means of such isolation interface.

According to International Patent Classification the invention is classified to H 03F 03/38.

The technical problem to be solved by the present invention is to find such a low price interface with a capacitive barrier and a method for transmitting a signal by means of such an isolation interface that between circuits at the input end and at the output end of the capacitive barrier even the fastest data transmission will be made possible, whereat

in the circuit at the input end a signal will be formed which will be the most appropriate input signal for the circuit at the output end and

the transmission will be insensitive to a very fast variation of the electrical potential difference, even in the range of 10 kV/μs, between the supplies of the said input and output circuits,
and at the same time the isolation interface with the capacitive barrier should be completed so that
the receiving circuit will pass to the right logical state immediately after its switching-on and
it will stay in the right state also when for a long time no change of the output signal of the circuit at the input end of the capacitive barrier has taken place.

An isolation interface renders possible data transmitting, normally in the digital form, between two or several circuits having separate supplying voltage sources. Since these circuits have no common mass connection, between them a voltage difference results, which may attain even a value of several kilovolts and may vary very fast so that the voltage difference variation rate attains the order of magnitude of 10 kV/μs.

In isolation interfaces the transient electrical currents between circuits are inhibited by means based on different physical principles.

The most common one is an optical isolation interface. An input circuit light emitting diode transforms an electrical signal into light pulses that are transformed by an output bipolar transistor back into an electrical signal. Except in the high-price range, the optical isolation interface makes possible only a relatively low data transmission rate on the level of several megahertz and the current consumption of said elements thereof is rather high.

A fast acceptance has been gained by an interface with a magnetic coupling between a magnetic loop and a magnetic field sensor. The magnetic unit can be advantageously

fabricated on a single substrate for an integrated circuit; the magnetic loop is a conductive track that is, through a silicon dioxide, separated from the elements that are connected to another voltage supply; the magnetic field sensor is a magneto-resistor. A data transmission at a rate up to 50 MHz is made possible. When appropriately constructed, its current consumption is lower than that of an optical isolation interface. However, it is fabricated according to a relatively pretentious technology since the magneto-resistor is added to the integrated circuit in demanding and high-cost technological steps.

There are also known isolation interfaces using a capacitive coupling. In a basic embodiment two opposite-in-phase digital output signals U1o±, being replicas of a transmitted input signal Ui, of an input circuit A1' are conducted to a first plate of either barrier capacitor C'± (Fig. 1). From their second plate digital input signals U2i± are conducted to an output circuit A2', at whose output a transmitted signal Uout appears. The high and low potential of a supplying voltage source for the input circuit A1' are U1+ and U1-, respectively, as well as U2+ and U2-, respectively, for the output circuit A2'. A second plate of either barrier capacitor C'± is through a capacitor C"± as well as through a resistor R'±, each of said connections representing a voltage divider, namely the first one for a time varying signal and the second one for a direct voltage signal, connected to a common potential of the supplying voltage source for the output circuit A2'. The time development of the input signal voltage Ui with regard to the said common potential is represented in a first window of Fig. 2; at $t = 90$ ns the potential difference between the supplying source for the first circuit A1' and the supplying source for the second circuit A2', resulting in a voltage on the capacitors C'+ and C'-, started to grow and reached the 50 V level. By a full line and a dashed line in a second and third window of Fig. 2 there are represented time developments of the opposite-in-phase digital signals U1o± and U2i±. In a fourth window of Fig. 2, however, the transmitted output signal Uout is represented, whose frequency is equal to the frequency of the input signal Ui. Direct and low-frequency potential differences

are limited in magnitude only by the break-down strength of the capacitors C'+ and C'-. The resistors R'± ensure that, as regards the magnitude, also at low frequencies the input signals U2i± are always within the range of allowed input voltages for voltage comparators in the circuit A2'. In numerous applications, however, the described interface must also function under fast variations of the potential difference between the supplying source of the first circuit A1' and the supplying source of the second circuit A2'. The necessary lowering of the high-frequency signals U2i± is reached by an appropriate ratio of the capacitances of the capacitors C'-, C''+ and C'-, C''-, respectively. This ratio must be 1:500 if the described interface should manage a voltage difference of 1 kV at a tolerated input voltage of 2 V for the voltage comparator. Such ratio, however, also lowers the amplitude of the signal replicas U2i± of the input signal Ui at the input to the circuit A2' to only a few millivolts. Hereby the signal transmission rate is retarded or even made impossible because the signal amplitudes are already in the range of characteristic offset voltages of a voltage comparator. Hence, if the insensitivity to a fast variation of the potential difference between the two supplying sources is ensured by the described interface it is not possible at the same time to ensure the fastest possible data transmission.

In the patent US 4,835,486 there is actually disclosed an interface provided with a capacitive coupling suitable for to a digital signal transmission up to the frequency of 1.5 MHz. A differentiating unit at the capacitive barrier is used, however, the time constant of the differentiating unit is 9 ns. So the time constant is longer than the characteristic time of variations of a signal replica at the output of a first circuit in front of the capacitive barrier and therefore the amplitude of the signal replica has to be limited by a diode limiter at an input of a circuit behind the capacitive barrier. Further, an input amplifier in the circuit behind the capacitive barrier transforms the signal pair into one single signal. Hereby the pulse width is additionally distorted since a complete symmetry in the amplifier output signal variation can never be provided for.

In the isolation interface with the capacitive coupling a limitation is immanent that no non-varying-in-time information can be transmitted thereby because of the capacitive barrier. Therefore after a switching-on or, when for a long time no change of the output signal of the circuit at the input end of the capacitive barrier has taken place, after a first change in the logical state of the output signal of the circuit at the output end of the capacitive barrier, the signal at the output end of the capacitive barrier is put into the right logical state, that is into the logical state of the said output signal.

The said technical problem is solved by an isolation interface with a capacitive barrier, comprising

- at the input end of the capacitive barrier, an input circuit with differential outputs for a first and a second logical output signals, respectively, that are replicas of a transmitted input signal and are complementary to one another,
- a first and a second barriers capacitor for the first and second logical signals, respectively,
- at the output end of the capacitive barrier an output circuit with inputs for a first and second logical input signal, respectively, that are complementary to one another, which output circuit comprises a first and a second voltage comparators,

the isolation interface of the invention with the capacitive barrier being characterized in

that in the input circuit a first and a second integrating units are provided, across which the first logical output signal and the second logical output signal, respectively, passed and by means of whose time constants the slope rates of the edges of the signals or the rising and falling-off times of the signals were adjusted,

and that to an output terminal of the first and the second barrier capacitors on the one hand and to a common potential terminal of the output circuit on the other hand such a first resistor and a second resistors, respectively, are connected,

that the time constant of a first differentiating unit made of the first barrier capacitor and of the first resistor
and the time constant of the second differentiating unit made of the second barrier capacitor and of the second resistor
are shorter than the rising and falling-off times of the logical output signals being the replicas of the transmitted signal.

The isolation interface of the invention with a capacitive barrier is further characterized in that the first logical input signal and the second logical input signal of the output circuit are conducted directly to a first and a second inputs, respectively, of the first voltage comparator as well as to a second and first inputs, respectively, of the second voltage comparator and that an output of the first voltage comparator and an output of the second voltage comparator are connected to inputs of a flip-flop, whose output is an output of the isolation interface with the capacitive barrier.

The isolation interface of the invention with a capacitive barrier is completed so that an input of the basic isolation interface invention with a capacitive barrier is connected to a control input of a pulse-width modulator, to whose second input a constant frequency signal is uninterruptedly conducted and whose output is connected to an input of an auxiliary isolation interface provided for transmission over an auxiliary communication channel, and that the output of the basic isolation interface with the capacitive barrier and an output of the auxiliary isolation interface for the transmission over the auxiliary communication channel are connected to inputs of a decision logical circuit that provides for a correct logical state of the signal transmitted by the basic isolation interface with the capacitive barrier and that an output of the decision logical circuit is the output of the isolation interface with the capacitive barrier.

The completed isolation interface of the invention with a capacitive barrier is further characterized in that individual output end units of the basic isolation interface with

the capacitive barrier are turned on or off depending upon the presence of the modulated signal at the output of the auxiliary isolation interface for the transmission over the auxiliary communication channel.

The said technical problem is also solved by a method for transmitting a signal through an isolation interface with a capacitive barrier, the method of the invention being characterized in that in an input circuit of the isolation interface with the capacitive barrier by means of the integration with an appropriate time constant the slope rates of the edges or the rising and falling-off times of signal replicas of the transmitted input signal are adjusted and that the said signal replicas are differentiated in a first differentiating unit and a second differentiating unit, respectively, of the capacitive barrier and that the time constants of the first and the second differentiating units are shorter than the rising and falling-off times of the signal replicas of the transmitted signal.

The method of the invention for transmitting of signal through the isolation interface with the capacitive barrier is further characterized in that signals of the derivatives generated in the differentiating units of the capacitive barrier are conducted directly to two voltage comparators comprised in an output circuit of the isolation interface with the capacitive barrier.

The completed inventive method for transmitting a signal through the isolation interface with the capacitive barrier is characterized in that, besides transmitting the input signal through a basic isolation interface with the capacitive barrier, there is uninterruptedly performed a transmitting of a constant frequency signal that is pulse-width-modulated by the transmitted input signal, through an auxiliary isolation interface for transmission over an auxiliary communication channel is performed and that, with regard to the modulation of the transmitted pulse-width-modulated signal,

the logical state of an output signal transmitted by the isolation interface with the capacitive barrier is adjusted.

The invention will now be disclosed in more detail and numerous advantages achieved will be presented by way of describing an embodiment of an isolation interface with a capacitive barrier and of a method performed by the said interface for transmitting a signal and with reference to the accompanying drawings and graphs representing in

Fig. 3 a schematic presentation of an isolation interface as completed by the invention, wherein to a basic isolation interface of the invention with a capacitive barrier a pulse-width modulator and an auxiliary isolation interface for transmitting a constant frequency signal that is modulated by an input signal are connected in order to transmit the information on the logical state of the transmitted signal;

Fig. 4 the time development of an input signal and the time development of signal replicas of the input signal as obtained by the isolation interface of the invention with a capacitive barrier, the said replicas having in front of a differentiating unit and behind it the edges with the slope rate of 1 V/ns, as well as the time development of an output signal;

Fig. 5 the time development of the same signals as in Fig. 4 with input signal replicas having the slope rate of 12 V/ns.

The basic isolation interface of the invention with a capacitive barrier is represented in a simplified form as a part of the circuit in Fig. 3. It comprises the following units.

- At the input end of the capacitive barrier an input circuit A1 with differential outputs for a first and a second logical output signals U1o+ and U1o-, respectively,that are replicas of a transmitted input signal Ui and are complementary to one another. In

the input circuit A1 a first integrating unit (R1, C1)+ and a second integrating unit (R1, C1)- are provided, across which the first logical output signal U1o+ and the second logical output signal U1o-, respectively, have passed. By means of the time constants of the integrating units (R1, C1)± the slope rates of the edges of the signals U1o± or the rising and falling-off times of the signals U1o± are adjusted.

- There follow a first barrier capacitor C+ and a second barrier capacitor C-, whereto the first logical signal U1o+ and the second logical signal U1o+ are conducted and to whose output terminal on the one hand and to a common potential terminal of an output circuit A2 on the other hand such first resistor R+ and second resistor R-, respectively, are connected that the time constant of a first differentiating unit (C+, R+) made of the first barrier capacitor C+ and of the first resistor R+, and the time constant of a second differentiating unit (C-, R-) made of the second barrier capacitor C- and of the second resistor R-, are shorter than the rising and falling-off times of the logical output signals U1o+ and U1o- being the replicas of the transmitted signal Ui. Hence, in the proposed isolation interface for transmitting a digital signal with the frequency up to 100 MHz the time constants of the first and the second differentiating circuits are of the order of magnitude 1 ns or even below. In the first differentiating circuit (C+, R+) the signal U1o+ is transformed into a signal U2i+ and on the second differentiating circuit (C-, R-) the signal U1o- is transformed into a signal U2i-. The signals U2i± are also complementary to one another.

- At the output end of the capacitive barrier an output circuit A2 with inputs for a first logical input signal U2i+ and a second logical input signal U2i-, respectively, is provided. The output circuit A2 comprises a first voltage comparator Co+ and a second voltage comparator Co-.

The high and the low potential of the supplying voltage source for the input circuit A1 are U1± and for the output circuit A2 there are U2±.

According to the invention the time constants of the integrating units (R1, C1)± are chosen so that the slope rates of the edges of the signals U1o± or the rising and falling-off times of the signals U1o± are adjusted in such a way that these times are longer than the time constants of the first and the second differentiating units, respectively, which, however, should be in the order of magnitude of 1 ns or even below.

Namely by controlling the slope rates of the edges of the output signals U1o± of the circuit A1, the amplitude and the time duration of the input signals U2i± of the circuit A2 are controlled. Out of the signals U1o± with lower slope rates of the edges, *e.g.* with the slope rate of 1 V/ns in Fig. 4, lower signals U2i± with a longer time duration arise. And the other way round, out of the signals U1o± with steeper edges, *e.g.* with the slope rate of 12 V/ns in Fig. 5, higher signals U2i± with a short time duration arise.

For the slope rates of 1 V/ns and 12 V/ns of the edges in Fig. 4 and 5, respectively, in the first two windows the time development of the input signal Ui and of the output signals U1o± of the circuit A1 and in the last two windows the time development of the input signals U2i± of the circuit A2 and of the output signal Uout of the circuit A2 are represented. At t=90 ns the potential difference between the supplying source of the first circuit A1 and the supplying source of the second circuit A2 started to grow and at t=150 ns reached the value of 50 V. The input signals U2i± of the circuit A2 (third window) consist of 50 mV pulses with the time duration of 10 ns for the slope rate of 1 V/ns of the edges of the signals U1o± (Fig. 4) and of approximately 600 mV pulses with the time duration of 1 ns for the slope rate of 12 V/ns of the edges of the signals U1o± (Fig. 5).

In the output circuit A2 the first logical input signal U2i+ and the second logical input signal U2i- are conducted directly to a first and a second inputs, respectively, of the

first voltage comparator Co+ as well as to a second and first inputs, respectively, of the second voltage comparator Co-.

An output of the first voltage comparator Co+ and an output of the second voltage comparator Co- are connected to inputs of a flip-flop F. The output of the flip-flop F is at the same time an output of the basic isolation interface of the invention with the capacitive barrier.

As shown above, with regard to the characteristics of the comparators Co± and also to the maximum speed of the data transmission as well as to the immunity from fast varying potential difference between the supplying sources of the circuits A1 and A2, the most favourable input signals U2i± for the output circuit A2 are generated.

The time constants of the differentiating units (C+, R+) and (C-, R-), however, are chosen with regard to the maximum variation rate of the potential difference between the voltage supplying sources of the circuits A1 and A2. If this maximum variation rate is 10 kV/µs, the dimensioning of the differentiating units must be such that the said varying potential difference results in direct voltages on the inputs of the circuit A2 lying within the range of values tolerable for this circuit. Namely, the amplitude of the signals U2i± depends only on the variation rate of the signals U1o± and not on their amplitude.

In the isolation interface of the invention with the capacitive barrier the circuit A2 is never overloaded by input signals U2i± since according to the invention their amplitudes and time durations can be altogether exclusively determined by just the rising times and the falling-off times of the signals U1o± and by the time constants of the first and the second differentiating units. However, in modern sub-micrometer technologies the signal variation rate is in the region from 1 V/ns to 10 V/ns. The time

constants of the differentiating units are strongly shortened and, preferably, they are below 1 nanosecond.

Since the amplitudes of the input signals U2i± are adjustable and therefore known, in the circuit A2 no amplifiers in front of the voltage comparators Co± are needed. This makes it possible that the pulse width is conserved from the circuit A1 to the circuit A2 extremely accurately, an error being below 0.5 ns, since the complementary signals U2i± are received by two equal comparators Co±, the first one sensing a transition from the state 0 into the state 1 and the second one sensing a transition from the state 1 into the state 0.

By the isolation interface of the invention with the capacitive barrier a digital data transmission up to the frequency of 100 MHz is rendered possible, which represents an improvement of the state of the art for two orders of magnitude.

By the isolation interface of the invention with the capacitive barrier two great problems of the data transmission have been solved:

- the isolation interface of the invention is immune from the fast variation in the order of magnitude of 10 kV/μs of the potential difference between the supplying voltage sources for the circuits A1 and A2 so that this potential difference variation is reflected on the input signals U2i± as a non-disturbing direct voltage contribution below 1 volt;
- just by the form of the mutually opposite in phase output signals U1o± of the circuit A1, the form of the input signals U2i± of the circuit A2 is determined.

In Fig. 3 the completed isolation interface of the invention with a capacitive barrier is represented, wherein, besides the basic isolation interface (A1, C+, C-, R+, R-, A2) of the invention with a capacitive barrier for fast data transmission over the basic channel

BCC, also an auxiliary isolation interface for transmission over an auxiliary communication channel (ACC) is comprised. As the auxiliary isolation interface there can be used the described isolation interface (A1, C+, C-, R+, R-, A2) of the invention with a capacitive barrier or an isolation interface with a lower attainable data transmission rate and therefore having a substantially lower electrical current consumption.

The input of the basic isolation interface (A1, C+, C-, R+, R-, A2) with the capacitive barrier is connected to a control input of a pulse-width modulator PWM, to whose second input a constant frequency signal, *e. g.* from an oscillator O, is uninterruptedly conducted. An output signal of the pulse-width modulator PWM modulated by the input signal Ui to be transmitted is conducted to an input of the auxiliary isolation interface provided for the transmission over the auxiliary communication channel ACC.

At the output of the auxiliary communication channel ACC an auxiliary output signal Uouta is uninterruptedly present. In this signal the ratio between the high logical level time duration and the low logical level time duration is not constant. If the input signal Ui is in the high logical level, the output signal Uouta, for example, has the high logical level in a longer period portion and the low logical level in a shorter period portion and the situation is reversed if the input signal Ui is in the low logical level. The always present data on the ratio between the durations of the high and the low logical levels of the constant frequency pulse-width-modulated signal Uouta represents an information on the logical state of the signal Ui at the input of the emitting part of the completed isolation interface with the capacitive barrier.

In this way the emitting part of the isolation interface conveys important additional information to the receiving part on the other side of the isolation barrier. Namely, the data receiving part, which is the main electrical current consumer in the receiving

circuit, can be turned off when the emitting part is not active, or the input of the receiving part is readjusted by means of the said information when the input signal Ui has not changed for a longer time, from 1 μs to 100 μs, or immediately after turning on the receiving part sets the right logical state of its own signal or initializes the output signal of the receiving part as soon as it has determined the logical state of the input signal Ui of the emitting part. Hence, to adjust the right logical state of the output signal in the receiving part of the completed isolation interface with the capacitive barrier it is not necessary to wait for the first change of the signal from the emitting part.

To this end the output of the basic isolation interface (A1, C+, C-, R+, R-, A2) with the capacitive barrier and the output of the auxiliary isolation interface for transmission over the auxiliary communication channel ACC are connected to inputs of a decision logical circuit DLC that provides for a correct logical state of the signal transmitted. The output of the decision logical circuit DLC is the output of the isolation interface with the capacitive barrier.

Claims

1. Isolation interface with a capacitive barrier, comprising

- at the input end of the capacitive barrier an input circuit (A1) with differential outputs for a first and a second logical output signals U1o+ and U1o-, respectively, that are replicas of a transmitted input signal Ui and are complementary to one another,

- a first barrier capacitor (C+) and a second barrier capacitor (C-) for the first and second logical signals U1o+ and U1o-, respectively,

- at the output end of the capacitive barrier, an output circuit (A2) with inputs for a first logical input signal U2i+ and a second logical input signal U2i-, respectively, that are complementary to one another, and the output circuit (A2) comprises a first voltage comparator (Co+) and a second voltage comparator (Co-), and

characterized in

that in the input circuit (A1) a first integrating unit (R1, C1)+ and a second integrating unit (R1, C1)- are provided, across which the first logical output signal U1o+ and the second logical output signal U1o-, respectively, passed and by means of whose time constants the slope rates of the edges of the signals U1o± or the rising and falling-off times of the signals U1o± were adjusted,

and that to an output terminal of the first barrier capacitor (C+) and of the second barrier capacitor (C-) on the one hand and to a common potential terminal of the output circuit (A2) on the other hand, such a first resistor (R+) and a second resistor (R-) are connected

that the time constant of a first differentiating unit (C+, R+) made of the first barrier capacitor (C+) and of the first resistor (R+)

and the time constant of the second differentiating unit (C-, R-) made of the second barrier capacitor (C-) and of the second resistor (R-)

are shorter than the rising and falling-off times of the logical output signals U1o+ and U1o- being the replicas of the transmitted signal Ui.

2. Isolation interface with a capacitive barrier as recited in claim 1, characterized in

that the first logical input signal U2i+ and the second logical input signal U2i- of the output circuit (A2) are conducted directly to a first and a second inputs, respectively, of the first voltage comparator (Co+) as well as to a second and first inputs, respectively, of the second voltage comparator (Co-)

and that an output of the first voltage comparator (C0+) and an output of the second voltage comparator (C0-) are connected to inputs of a flip-flop (F),

whose output is an output of the isolation interface with the capacitive barrier.

3. Isolation interface with a capacitive barrier as recited in claim 1 or 2, characterized in

that an input of the basic isolation interface (A1, C+, C-, R+, R-, A2) with a capacitive barrier is connected to a control input of a pulse-width modulator (PWM), to whose second input a constant frequency signal is uninterruptedly conducted and whose output is connected to an input of an auxiliary isolation interface provided for transmission over an auxiliary communication channel (ACC),

that the output of the basic isolation interface (A1, C+, C-, R+, R-, A2) with the capacitive barrier and an output of the auxiliary isolation interface for transmission over the auxiliary communication channel (ACC) are connected to inputs of a decision logical circuit (DLC) that provides for a correct logical state of the signal transmitted by the basic isolation interface (A1, C+, C-, R+, R-, A2) with the capacitive barrier,

and that an output of the decision logical circuit (DLC) is the output of the isolation interface with the capacitive barrier.

4. Isolation interface with a capacitive barrier as recited in claim 3, characterized in

that individual output end units of the basic isolation interface (A1, C+, C-, R+, R-, A2) with the capacitive barrier are turned on or off depending upon the state of the modulated signal at the output of the auxiliary isolation interface for the transmission over the auxiliary communication channel (ACC).

6. Method for transmitting a signal through an isolation interface with a capacitive barrier, characterized in

that in an input circuit of the isolation interface with the capacitive barrier by means of an integration with an appropriate time constant the slope rates of the edges or the rising and falling-off times of signal replicas U1o+ and U1o- of the transmitted signal Ui are adjusted

and that the said signal replicas U1o+ and U1o- are differentiated in a first differentiating unit and in a second differentiating unit, respectively, of the capacitive barrier,

and that the time constants of the first and the second differentiating unit are shorter than the rising and falling-off times of the signal replicas U1o+ and U1o-, respectively, of the transmitted signal Ui.

7. Method for transmitting a signal through an isolation interface with a capacitive barrier as recited in claim 6, characterized in

that signals U2i± of the derivatives performed in the differentiating units of the capacitive barrier are conducted directly to two voltage comparators comprised in an output circuit of the isolation interface with the capacitive barrier.

8. Method for transmitting a signal through an isolation interface with a capacitive barrier as recited in claim 6 or 7, characterized in

that, besides transmitting the input signal Ui through the basic isolation interface with the capacitive barrier, there is uninterruptedly performed the transmitting of a constant frequency signal Uia, which is pulse-width-modulated with the input signal Ui,

through an auxiliary isolation interface for transmission over an auxiliary communication channel (ACC)

and that according to a modulation of the transmitted pulse-width-modulated signal Uouta, the logical state of an signal Uout transmitted by the isolation interface with the capacitive barrier is adjusted.

ABSTRACT OF THE DISCLOSURE

A transmission of a signal through an isolation interface with a capacitive barrier is performed so that in an input circuit of the interface by integrating with an appropriate time constant the slope rates of the edges of signal replicas U1o± of the transmitted signal are adjusted and that the said signal replicas are differentiated either in an appropriate differentiating unit, whereat the time constants of these differentiating units are shorter than the rising and falling-off times of the signal replicas and are advantageously in the order of magnitude of 1 nanosecond or below. Therefore, in a circuit on the output side of the capacitive barrier no amplifier in front of voltage comparators is needed, which makes it possible that the pulse width is maintained extremely precisely. The data transmission is immune from the fast variation in the order of magnitude of 10 kV/μs of the potential difference between the voltage supplying sources for the input and the output circuits. By the invention a digital data transmission up to the frequency of 100 MHz is rendered possible.

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I, the undersigned Vera Lamut, Permanent Court Interpreter for the German and English languages, appointed by the decree of the Secretariat of Justice and General Administration of the Socialist Republic Slovenia in Ljubljana No. G.Z. P 74/A-9/71 of 14 September 1971, do hereby certify that the attached English translation is, to the best of my knowledge and belief, a true and correct translation of the priority document P-200300001.

Ljubljana, 30 September 2003

Vera Lamut